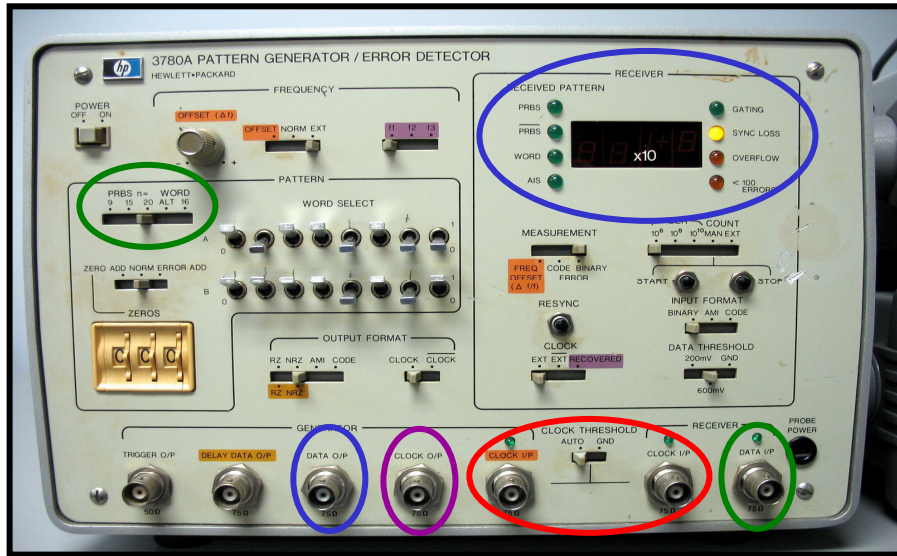# HP 3780A Bit Error Rate Tester (BERT)

Quick Reference Guide

Overview

- The (somewhat old) HP 3780A consists of a serial data generator, a data-receiver with synchronization capabilities, comparison circuitry to look for differences between the generated and received data sequences (error detector), and an LED display to show bit error rate (BER).

- The data generator can output either a pseudo-random-bit-sequence (PRBS), or a user-specified 16 bit pattern (continually repeated), in non-return-to-zero (NRZ) format. Additional options include RZ and other special formats, ability to insert zeros into the sequence to test clock recovery performance, and ability to intentionally insert errors to check that the receiver display is operating properly.

- The data receiver can be configured to count for 10^6, 10^8, or 10^{10} bits before displaying the result. Generally 10^6 is enough unless you are looking for very low rates (10^{-6} and below).

Main Controls and I/O Connectors

I/O Connectors

1. **Data O/P** This is the serial data output. It outputs TTL levels (0 to 4V), and must be converted with external circuitry if other levels (e.g. bipolar for input to a mixer) are desired.

2. **Clock O/P** This is a companion clock output waveform. It can be connected to the Clock I/P connector in the receiver section, or left open (if your device has its own clock recovery).

3. **Clock I/P** There are two of these. In the Generator section, this accepts an external clock to allow you to control the data rate with an external squarewave signal (TTL). In the receiver, it is used for bit sampling during the error detection.

4. **Data I/P** This is where you should input the received data. Be sure to set the DataThreshold to match your voltage levels (600 mV for TTL/CMOS, or GND for mixer output).

Controls and Display

1. **Default Setup** There is no microprocessor in the instrument, so there is no simple default button. **Set the controls as shown in the picture above.**

2. **Data Selector** Controls whether a PRBS is output, or the 16 bit pattern defined by the switches is used.

3. **Data Display** Show the error rate after a block of bits has been received. The various LEDs surrounding the display provide status such Gating (measurement in progress) and Sync Loss (data waveform not received or too corrupted to synchronize to)
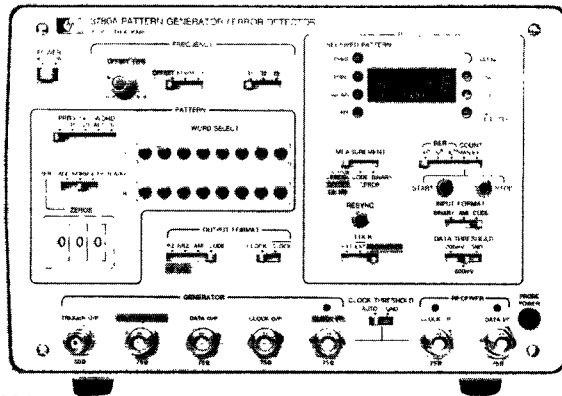
TELECOMMUNICATIONS TEST EQUIPMENT
PCM/TDM Error Measuring Set & Digital Transmission Analyzer
Models 3780A, 3764A

HP 3780A
- Easy-to-use portable unit
- Binary and code error measurements
- Clock frequency offset generation and measurement
- Ternary coded and binary interfaces
- Data logging and graphs to external printer

HP 3780A
Option 001

HP 3764A
- Error analysis at 2, 8, 34 & 139 Mbit/s based on latest G.821 Recommendation or error & jitter measurement and analysis at 139 Mbit/s only
- Powerful data logging facilities
- Single key measurement set-up using preset memory
- Portable single-unit construction

HP 3764A

DESIGNED FOR **HP-IB** SYSTEMS

HP 3780A Pattern Generator/Error Detector

The HP 3780A Pattern Generator/Error Detection is a Comprehensive error measuring set in one portable package for use in manufacturing, field trials, commissioning and maintenance of digital transmission terminal and link equipment.

The instrument measures binary errors and code errors in digital transmission equipment operating at rates between 1 kb/s and 50 Mb/s. Frequency offset generation and measurement are provided at the standard PCM/TDM transmission rates.

A range of standard PRBS test patterns and automatic pattern recognition/synchronisation are provided for simple performance checks. It also has flexible WORD generation and zero substitution to explore regenerator timing recovery performance and detect systematic errors.

Binary clock and data or ternary coded data interfaces can be selected with automatic equalisation at 2, 8 and 34 Mb/s on the Receiver.

Results are displayed as error COUNT or BER over a range of gating periods, and can be logged or presented graphically on an external printer.

Ordering Information

	Price
HP 3780A Standard: internal fixed rates of 2048, 8448 & 1536 kb/s; HDB3/HDB2 ternary coding.	$8,200
Option 232: RS-232 printer port replaces BCD printer and plotter outputs.	NC

Frequency/Ternary coding Options

	Price
Option 100: internal fixed rates of 2048, 8448 & 34368 kb/s; HDB3/HDB2 ternary coding.	$235
Option 101: internal fixed rates of 1544, 6312 & 44736 kb/s; B6ZS/B3ZS ternary coding.	NC
Option 102: internal fixed rates of 1544, 6312 & 3152 kb/s; B6ZS/B3ZS ternary coding.	NC
Option 103: internal fixed rates of 2048, 8448 & 34368 kb/s; 2 23-1 PRBS replaces 2 9-1; HDB3 ternary coding.	$550
Option 104: as option 103 but with Siemens 1.6 mm connectors.	$600

Frequency Offset Option

	Price
Option 099: frequency offset measurement only, frequency offset generation deleted.	−$165

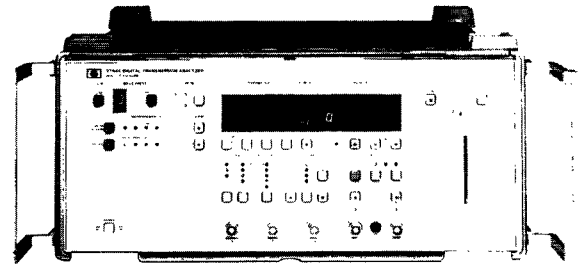### Word/Connector Options

	Price
Option 001: all words replaced by a 16 bit front panel programmable word.	$230
Option 002: Siemens 1.6 mm connectors.	$85
Option 003: options 001 and 002 combined.	$290

HP 3764A Digital Transmission Analyzer

The HP 3764A Digital Transmission Analyzer is available in three versions. The standard instrument offers a low-cost solution to users who want to perform error measurements at 139 Mbit/s only. The option 001 instrument is a multirate error analyzer in a single, rugged, low-weight case particularly suited to field installation and maintenance applications. The option 002 instrument performs a full set of bit error and jitter measurements at 139 Mbit/s to match development or manufacturing requirements.

Specifications Summary
Generator Section

Clocks: Standard & Opt 002, 139.264 MHz with fixed frequency offsets; Opt 001, 139.264, 34.368, 8.448 & 2.048 MHz, with fixed frequency offsets available as Opt 005.

Data outputs: CMI format at 139 Mbit/s; HDB3 format at 34, 8 & 2 Mbit/s; binary-RZ from 1 to 150 Mbit/s, NRZ from 1 to 170 Mbit/s (using external clock source), ECL levels, 75 ohm unbalanced.

Data patterns: PRBS 2^{15}-1 and 2^{23}-1; word, programmable 16-bit or two alternating 8-bit words; errors, single error or fixed 1 x 10^{-3} rate.

Receiver Section

Recovered clock: 139.264 Mbit/s ± 3 Mbit/s; 34, 8, 2 Mbit/s ± 100 ppm.

Binary clock: 1 kHz to 170 MHz.

Data inputs: 75 ohm terminated; monitor (25 dB additional gain); binary, RZ or NRZ, ECL levels.

Error analysis: Error count, error ratio, error seconds, error-free seconds, % unavailability, % errored seconds, % severely-errored seconds, % degraded minutes. All measurements made simultaneously and in accordance with Recommendation G.821.

Jitter analysis: Peak-to-Peak, hit count, hit seconds, hit-free seconds. Further analysis possible using internal jitter filters and demodulated jitter output.

Internal printer: Any combination of analysis parameters can be selected for printing.

Ordering Information

	Price
HP 3764A Standard: Error analysis at 139 Mbit/s.	$10,400
Option 003: Standard with 3 additional delayed outputs.	$800
Option 002: Error & jitter analysis at 139 Mbit/s.	$2,800
Option 001: Error analysis at 2, 8, 34 & 139 Mbit/s.	$820
Option 005: Multirate fixed-frequency offsets for Option 001.	$1,400
Option 010: Tape cartridge unit replaces the printer.	NC